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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,416	07/11/2003	Terry P. Borer	ALT.P021	7068

27296 7590 06/08/2006

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/618,416	BORER ET AL.	
	Examin r	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communicati n appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4 and 28* is/are allowed.

6)☒ Claim(s) *1-3,5-8,12-17,19,21-23,25-27 and 29-31* is/are rejected.

7)☒ Claim(s) *9-11,18,20,24,32 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/618,416 and amendment filed on 4/10/2006. Claims 1-33 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-8, 12-17,19, 21-23, 25-27 and 29-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Fung et al. (6,871,328).

4. As to claims 1, 12 and 25, Fung et al. teach a method for implementing a user logic design in a programmable logic device (PLD) or implementing logic design memory in physical memory devices of a PLD using placing and routing tools (Fig. 1 & 6 and its description). The placing and routing tools (EDA tool) is shown in Fig. 1. The EDA tool determines a first location on the PLD to place a user defined logic region in response to user specified constraints for placement of the user defined logic region (the placement and routing tools map one of user defined logic regions 908, 910 and 912 into one of locations 902, 904 and 906 of target devices in PLD 900 according to user defined constraints). The placement and routing tools also place said one of user defined logic regions 908, 910 and 912 into other one of locations 902, 904 and 906 of

target devices in PLD 900 when it is applicable according to other user defined constraints (independent of the user defined constraints for placement) (Fig. 9). In addition, the invention as taught by Fung et al. provides a way to optimize how logic design memory (user logic design) is implemented in physical memory devices. A logic design to hardware application implements a user logic design in a programmable logic device. The logic design to hardware application implements logic design memory defined in the user logic design in physical memory devices on the PLD. The logic design to hardware application dynamically considers the target PLD and may derive all corresponding constraints accordingly. All user constraints and physical constraints are taken into account when determining an implementation and any solution is guaranteed to satisfy all such constraints. The logic design to hardware application may initially map the logic design memory onto the physical memory devices of the representation of the target PLD. The mapping may then be optimized by moving segments of the logic design memory between the physical memory devices. A simulated annealing process is performed by moving memory slices between physical memory devices in search of a more efficient solution. The moving process changes locations from a first location to a second location. The resultant mapping from the optimization may then be implemented in the PLD by placing and routing the memory blocks, corresponding to the mapped memory slices, in the physical circuit (see summary). The user constraints may include region constraints and floating region constraints (i.e., specifying region constraints or relative locations within the PLD to implement particular logic design memory) or any other suitable constraint. It is feasibility-driven because the analysis

involved may, for the most part, be directed towards obtaining a solution that satisfies all constraints. The solution need not be optimized (col. 5, lines 25-58). The floating region constraint (described in col. 5 line 59 to col. 6 line 15) is the same as soft constraint as recited in claim 12. These teachings mean that the placing and routing tools (EDA tool) determine a first location on the PLD to place a user defined logic region in response to user specified constraints for placement of the user defined logic region and then the placement and routing tools determine a second location to place the user defined logic region, wherein the second location is determined independent of the user specified constraints for placement.

5. As to claim 19, remarks set forth in rejection claims 1, 12 and 25 equally apply. Fung et al. teach a method for implementing a user logic design in a programmable logic device (PLD) using placing and routing tools (Fig. 1 & 6 and its description). It is noted that the placing and routing tools would perform both placement and routing on the PLD based in user defined constraints. The user defined constraint include region constraints and floating region constraints (i.e., specifying regions or relative locations within the PLD to implement particular logic design), physical memory device type constraints (e.g., user specifies particular physical memory device type to user), and any other suitable constraint (col. 5 lines 42-58). The other suitable constraint would be user specified routing constraints when routing process is performed. The invention as taught by Fung et al. provides a way to optimize how logic design memory (user logic design) is implemented in physical memory devices (col. 2 lines 23-26) (this suggests providing routing strategies when routing process is performed). The implementation of

user logic design in physical memory devices would include placement and routing of the user logic design. Fung et al. teach different physical constraints and characteristics of the different physical memory devices and their layout on the particular target PLD may be one of the factors in determining the feasibility of a particular mapping. Other factors may include constraints defined by user, and the layout of all other elements, such as logic array blocks, throughout the PLD (e.g., in anticipation of routing) (col. 5 lines 25-40). The user defined constraints as taught by Fung would include user specified routing constraints that pertain to categories of routing resources to use. In order to meet specified routing constraints, routing strategies must be required. It is a common practice to layout routing strategies before perform routing process. Routing resources are required and must be specified for different routing categories (e.g. power wiring, signal wire, global routing, detailed routing…). Fung et al. teach performing feasibility-driven analysis because the feasibility-driven analysis involved may be directed towards obtaining a solution that satisfies all constraints (user defined region constraint and floating region constraints) (at least see col. 5 lines 42-58). Note the user defined region constraints include constraints for placement and routing. These teachings suggest another routing strategies independent of the user specified routing constraints are determined and provided to routing tool in order to obtain the solution that satisfies all constraints.

6. As to claim 21, remarks set in rejection claim 19 apply. The logic design to hardware application implementation based on user defined constraints, floating region constraints and any other constraints (routing constraints must be included because

Fung et al. placement and routing process) (col. 5-6) as taught by Fung et al. would suggest the placing and routing would select resources for the user specified signal on the PLD independent of the user specified routing constraints in order to obtain an optimal solution that satisfies all constraints.

7. As to claims 2-3 and 26-27, Fung et al. teach the logic design to hardware application may first perform a greedy, feasibility-driven analysis to implement the logic memory in available physical memory devices of the target PLD in view of physical constraints of the physical memory devices, user constraints and other such constraints. The user constraints may include region constraints and floating region constraints (i.e., specifying region constraints or relative locations within the PLD to implement particular logic design memory) or any other suitable constraint. It is feasibility-driven because the analysis involved may, for the most part, be directed towards obtaining a solution that satisfies all constraints. The solution need not be optimized (col. 5, lines 25-58). The floating region constraint is described in col. 5 line 59 to col. 6 line 15. This feasibility-driven solution may then be modified as a result of an optimization analysis. During optimization, the logic design to hardware application may redistribute memory slices between the physical memory devices to which they were assigned. The focus is to gather related logic together, balance the use of each physical memory device, optimize timing, and consolidate memory slices that are part of the same floating region (see Fig. 6 description). These teachings mean that the placing and routing tools determine the second location is performed in response to the first location not satisfying design parameters and the placement and routing tools determine the second

location is performed in response to the first location not satisfying the user specified constraints.

8. As to claims 22-23, remarks set forth in rejection claim 2-3 equally apply. Because Fung et al. teach using placing and routing tools to implement the logic design to hardware application based on user defined constraints, floating region constraints and any other constraints in order to obtain an optimal solution for all constraints, the teachings of Fung et al. would suggest the claimed limitations regarding performing routing as recited in the claims.

9. As to claims 5 and 29, Fung et al. teach the logic design to hardware application may first perform a greedy, feasibility-driven analysis to implement the logic memory in available physical memory devices of the target PLD in view of physical constraints of the physical memory devices, user constraints and other such constraints (floating region constraint, routing constraint…). The user constraints may include region constraints and floating region constraints (i.e., specifying region constraints or relative locations within the PLD to implement particular logic design memory) or any other suitable constraint. It is feasibility-driven because the analysis involved may, for the most part, be directed towards obtaining a solution that satisfies all constraints. The solution need not be optimized (col. 5, lines 25-58). The floating region constraint is described in col. 5 line 59 to col. 6 line 15. This feasibility-driven solution may then be modified as a result of an optimization analysis. During optimization, the logic design to hardware application may redistribute memory slices between the physical memory devices to which they were assigned. The focus is to gather related logic together,

balance the use of each physical memory device, optimize timing, and consolidate memory slices that are part of the same floating region. The optimization is performed by a simulated annealing process based on cost function (see Fig. 6 description at least col. 16). These teachings clearly suggest the claimed limitation of determining the second location in response to a triggering event.

10. As to claims 6-7 and 30, Fung et al. teach using placing and routing tools to place determine positions to place components (slices, components, circuit elements) within the user-defined logic regions on the target device (at least col. 2 lines 25-60, col. 3 lines 1-37; col. 5 lines 1-67, col. 6 lines 1-67). Fung et al. teach that if the logic design to hardware application determines that mapping has succeeded, the logic design to hardware application may perform simulated annealing based on cost function on the solution to explore other possible solutions for optimization purposes (Fig. 6, col. 6).

11. As to claims 8 and 31, Fung et al. teach relax user's constraints (col. 16 lines 1-8). The relax user's constraints is the same as remove constraints.

12. As to claims 13, 15, 16 and 17, Fung et al. teach using placing and routing tools to determine first location for placing the user defined logic region by assigning an initial location for user defined logic regions, moving the user defined logic region to a new location and evaluating a cost function associated with the user defined logic region in the new location (Figs. 1, 6 and its description, col. 5, 6, 16).

13. As to claim 14, Fung et al. the feasibility-driven solution may then be modified as a result of an optimization analysis. The focus is to gather related logic together, balance the use of each physical memory device, optimize timing, and consolidate

memory slices that are part of the same floating region (col. 6) and determining routing resources requirements (col. 16, the failures are due to insufficient resources including resources for placement and routing).

Allowable Subject Matter

14. Claims 4 and 28 are allowed over the prior art of record.

15. Claims 9-11, 18, 20, 24, and 32-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach or fairly suggest removing constraints associated with the user-defined logic regions; determining routing resources to allocating to user specified signals on the target PLD in response to user specified routing constraints; selecting routing resources for a non-user specified signal on the PLDs without utilizing the user specified routing constraints; determining additional routing strategies for routing the signals is performed in response to a threshold number of routing strategies being determined; and the EDA tool determines the second location is performed in response to having a threshold number of options generated.

Remarks

16. Note: PTOL-326 filed on 1/11/06, box 6 has been corrected as --Claim(s) 1-3, 5-8, 12-17, 19, 21-23, 25-27 and 29-31--; box 7 has been corrected as –Claim(s) 4, 9-11, 18, 20, 24, 28 and 32-33--. The applicant's remarks have been considered, but they are persuasive. Applicants did not specifically answer to specifically question raised by

Examiner to clearly point out where in the specification and drawing each claimed limitation is described in the independent claims, but generally refer to Figures 13, 16-17, and pages 4 and 17-29. Applicant did not specifically point out page and lines numbers. Fung et al. anticipated the claimed limitations. Fung et al. teach user placement constraints (col. 6 lines 59-67; col. 7 lines 1-4); user constraints (col. 2 lines 26-37; col. 3 lines 1-27). Fung et al. mapping user-created logic design (e.g. logic design memory defined by user) into physical memory devices on a programmable logic device (col. 4 lines 29-44). The user defined memory comprising memory slices, where memory slices are grouped together into logic group based on user defined constraints (one or more constraint sub-group); constraint sub-groups and cliques of each compatible logic group are sorted according to appropriate parameters, criteria or both and the constraints sub-groups may re-sorted based on the information regarding to the failure (col. 3 lines 1-27). Therefore, Examiner disagrees with Applicants that cliques are not user defined logic regions. Examiner submits that at least Fung et al. teach user logic design (col. 2 lines 26-37), where the user logic design comprising memory device, memory slices and cliques that are placed on the PLD based on user defined placement constraints (see summary, col. 6 lines 59-67; col. 7 lines 1-4). Fung et al. teach floating regions, floating region constraints, user constraints (col. 5 lines 25-67 col. 6 lines 1-4). If the mapping of all memory slices is successful, the logic design to hardware application may optimize by performing a simulated annealing process in which memory slices are moved between physical memory devices in search of a more efficient solution. The resultant mapping from the optimization by then be implemented in the

programmable logic device (PLD) by placing and routing the memory blocks, corresponding to the mapped memory slices in the physical circuit. Note that Fung et al. user defined placement constraints (col. 6 lines 59-67; col. 7 lines 1-4). Since Fung et al. both placement and routing (col. 3 lines 27-37). Since Fung et al. placement includes user defined constraints, the routing must also include user routing constraints and routing strategies which must be used during routing process. In addition, Fung et al. teach floating region that is corresponding to user defined logic region as claimed because the floating region can be floated any where on the PLD and the sizes are flexible and fixed (col. 5 lines 15-67; col. 6 lines 1-14). Note that floating regions are moved from one place (first location) to another place (second location) based on user constraints. User constraints include region constraints and floating region constraints (col. 5 lines 42-58). Therefore, placement of these floating regions are independent of user defined constraints. The same reasons apply to routing process.

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vote Seek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vote Seek

VUTHE SIEK
PRIMARY EXAMINER